⇒ Conversion of NAND ckt. into OR, AND & NOT circuits:

A NAND-gate can be used to build an OR, AND, or a NOT ckt. when all inputs of a NAND gates are connected together a NOT-gate results shown in fig. 6(a), because if $A=1$, the output of a NAND gate is $\overline{A}.\overline{A} = \overline{1}.\overline{1} = \overline{1} = 0$ and if $A=0$, the output is $\overline{A}.\overline{A} = \overline{0}.\overline{0} = \overline{0} = 1$.

Fig. 6(a) NOT-gate from NAND gate.

→ **AND CKT:-** A NAND-gate followed by NOT ckt is an AND gate. shown in fig. 6(b).

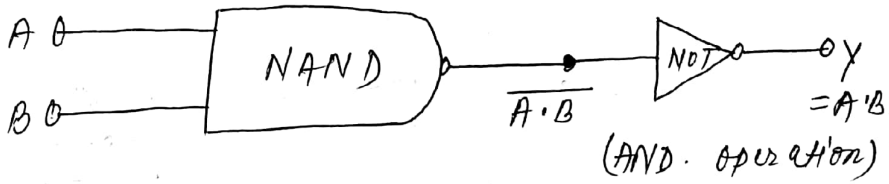


Fig. 6(b): AND from NAND & NOT.

AND-gate can also be obtained by using two NAND-gates repeatedly fig. 6(a). The output of two inputs NAND-gate is fed to single input.

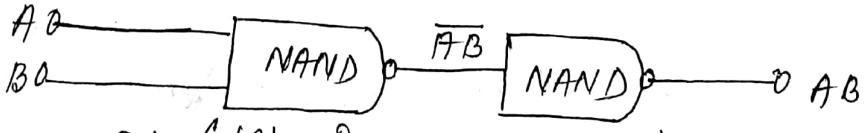


Fig. 6(c) Double NAND's is a AND.

In NAND-gate, Hence

$\overline{\overline{A}\,\overline{B}} = A\,B$ which is output of an AND-gate.

→ **OR-Ckt:-** OR-gate fig 6-(d) from NAND gate is obtained by using two single input NAND gates and one, two inputs NAND gate.

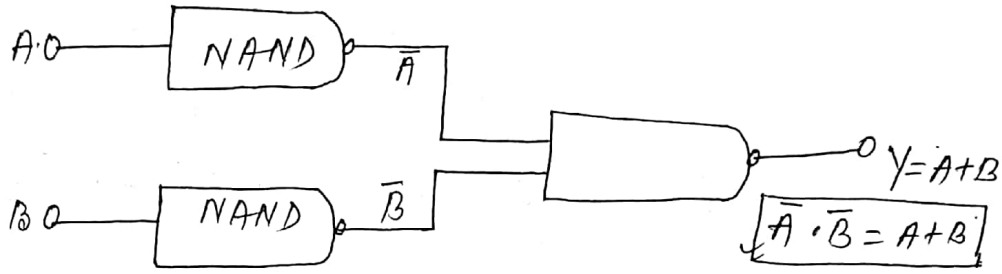


Fig - 6-(d).

First two NAND's convert A & B into $\overline{A}$ & $\overline{B}$. The 2nd two inputs NAND gives $\overline{A}\cdot\overline{B} = \overline{\overline{A}}+\overline{\overline{B}}$ $= A+B$, which is OR-gate. OR-gate can also be obtained by connecting two NOT-output to two inputs of a NAND ckt. shown fig. 6(e).

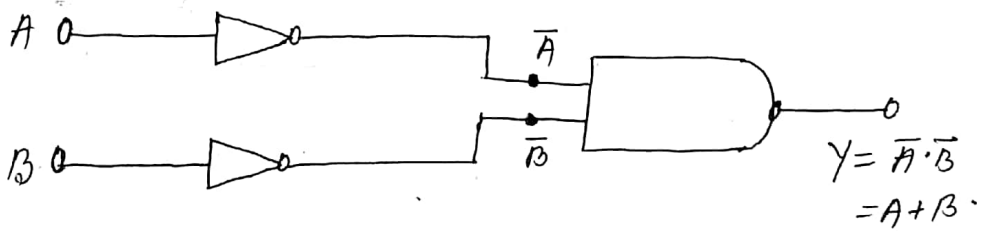


Fig - 6-(e) OR-gate from 1 NANDs two NOT.

→ **EX-OR Ckt [FROM NAND CKT]:-**

The exclusive OR gate (called XOR-gate) is a two input gate having an output in state 1 if either A or B but not

both is in state 1. $Y = A \oplus B$.

TRUTH TABLE FOR XOR-Gate:

Input A	Input B	output $Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

XOR SYMBOL:-

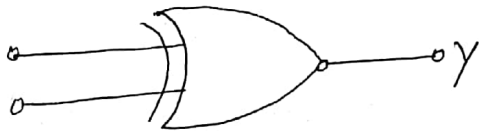
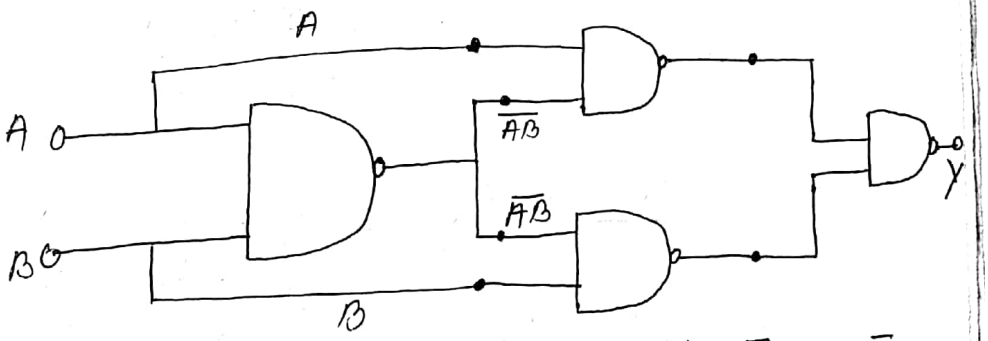


Fig. 6(f).

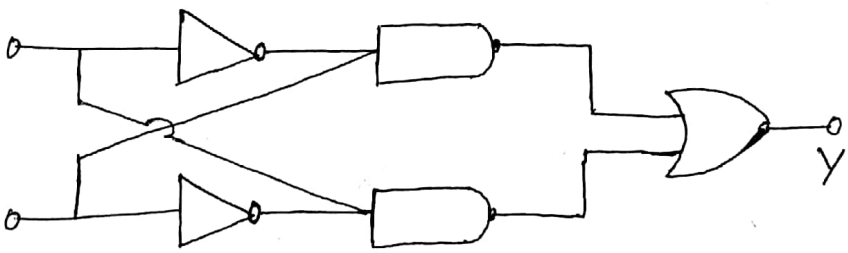
It is a combination of AND, OR & NOT gates.

using four NAND gates XOR can be obtained as follows:-



$Y = \bar{A}B + A\bar{B}$

Fig. 6(g) XOR-gate from 4 NAND's



$Y = \bar{A}B + A\bar{B}$
$= A\bar{B} + \bar{A}B$.

Fig. 6(h)

↓ It is a combination of AND, OR & NOT gates.